Design of a High-Efficiency GaN High-Electron Mobility Transistor Microwave Power Amplifier

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Abstract

This study presents a design procedure to obtain high-efficiency for microwave power amplifier. The designed amplifier uses a GaN high electron mobility transistor as an active device. Matching networks including input and output networks are realized using Megtron6 substrate microstrip lines. The designed amplifier operates at 2.1 GHz band. The simulated results show that the amplifier delivers a maximum power-added efficiency of 73.2% at output power and power gain of 47.8 dBm and 13.8 dB, respectively. This promising designed performance makes this amplifier to be an excellent candidate for use in modern wireless communication systems like radar, mobile network, and satellite communications.

Keywords: Microwave engineering, power amplifier, GaN, HEMT

1. Introduction

Microwave solid-state power amplifiers (SSPAs) are key components in various recent wireless communications systems like very small aperture terminal (VSAT) satellite communications, wireless LAN (WLAN), RFID, phased array radar and cellular networks or in broadcasting systems like terrestrial electronic and in other important applications like electronic warfare. One key requirement for the SSPAs is high-efficiency operation. The reason is that SSPA is the component consuming most of the system power. There exist various techniques to enhance the efficiency of the SSPA including common classes of operation such as D, E and F [1-3] or using harmonic tuning approach [4]. For the class-D, H. Kobayshi et al. in [5] designed a high efficiency SSPA using current-mode class-D. This SSPA achieves 76.3 % power-added efficiency (PAE) at 290 mW power output and 71.3 % PAE at 870 mW output power using GaAs field-effect transistor (FET) at an operation frequency of 900 MHz. T. Mury *et al.* in [7] proposes a class-E SSPA based on a GaAs metal semiconductor field effect transistor (MESFET) technology. The SSPA was fabricated and tested at 2.41 GHz and the matching networks of this type of SSPA is designed to treat up to the third harmonic but without using any compensation techniques. This SSPA achieves a peak PAE of 60% and drains efficiency of 69%. However, it has been shown that the class E SSPA has lower power output capability compared with that of the class-F SSPA at the same frequency band. As presented in [10, 11], SSPAs using a class-F approach which is based on GaN high-electron mobility transistor (HEMT) technology deliver PAE and drain efficiency of more than 70% at C-band and S-band while the output power is on the order of 30 dBm. The only downsize of the class-F compared with the class-E is its matching network is more complicated. To overcome the complexity of the matching networks as incorporated in the class-E and class-F, this paper aims to use a harmonic termination method. This approach is realized by using harmonic termination networks to suppress the harmonics. It is based on a source/load-pull technique which can be implemented using a mechanical tuner or running simulation on large-signal model of the active devices. The main advantage of the harmonic termination approach over the class-E and class-F ones is that its input/output harmonic treatment networks are relatively simpler. This also helps to reduce the circuit size of the SSPAs. This paper aims to design a GaN HEMT SSPA operating at 2.1 GHz with high efficiency and high output power. The rest of the paper is organized as follows. Section 2 presents details in design procedure of the SSPA. Section 3 presents and discusses the simulated results and finally Section 4 will conclude the paper.

2. Design procedure

The harmonic termination method for high-efficiency operation can be expressed through the following equations:

$$v_{\mathrm{DS}}(t) = V_0 + \sum_{\mathrm{n}=1} \sqrt{2} V_{\mathrm{n}} \sin(\mathrm{n}\omega_0 t + \phi_{\mathrm{n}}) \quad (1)$$

$$i_{\mathrm{DS}}(t) = I_0 + \sum_{\mathrm{n}=1} \sqrt{2} I_{\mathrm{n}} \sin(\mathrm{n}\omega_0 t + \phi_{\mathrm{n}} + \psi_{\mathrm{n}}) \quad (2)$$

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where $v_{\mathrm{DS}}(t)$ and $i_{\mathrm{DS}}(t)$ are time-dependent voltage and current at the drain terminal of the transistor; V_0 and I_0 are DC components of the $v_{\mathrm{DS}}(t)$ and $i_{\mathrm{DS}}(t)$, respectively; ω_0 is the operation frequency while ϕ_{n} and ψ_{n} are phase parameters.

From this, the average power dissipation on the transistor can be calculated as:

$$P_{\mathrm{a}} = \frac{1}{T}\int_0^T v_{DS}(t) i_{DS}(t) dt = V_0 I_0 + \\ + \sum_{\mathrm{n=1}} V_0 I_0 \cos\psi_{\mathrm{n}} \quad (3)$$

This means to minimize power dissipation on transistor or maximize the efficiency, two following conditions must be fulfilled simultaneously:

$$V_0 I_0 + V_1 I_1 \cos\psi_1 = 0 \quad (4)$$

$$\sum_{\mathrm{n=2}} V_{\mathrm{n}} I_{\mathrm{n}} \cos\psi_{\mathrm{n}} = 0 \quad (5)$$

Condition (4) means all DC supplied power is converted to the fundamental output signal power while condition (5) implies that all harmonics must be suppressed. In this paper, we fulfill these conditions by using a load/source pull technique which is embedded in a Keysight ADS 2011.01 simulator. This study uses a GaN HEMT supplied by Cree company as an active device of the SSPA. The SSPA operates in a deep class-AB mode with the following bias condition: V_{GS} = -2.7 V; V_{DS} = 34 *V*. Where V_{GS} and V_{DS} are gate-to-source and drain-to-source voltages, respectively. The next step is to find out optimum input/output impedances to fulfill conditions (4) and (5) as mentioned. Table 1 gives the values of optimum load (Z_L) and source (Z_S) impedances found out by running the load/source pull simulation in ADS.

Table 1. Values of optimum impedances

Source impedance		Load impedance		
2.1 GHz	*4.2 GHz*	*2.1 GHz*	*4.2 GHz*	*6.3 GHz*
1.2 + j2.1 Ω	1 + j10 Ω	2.7 + j3.5 Ω	1 – j14 Ω	1 – j1.2 Ω

It can be seen in the table that, the optimum second harmonic impedances locate around the boundary of the Smith chart indicating a phase difference of ±π/2 between voltage and current at the drain terminal of the transistor satisfying condition (5). Condition (4) for the fundamental frequency is satisfied with the above optimum fundamental impedances at 2.1 GHz. The initial performance of the amplifier which is obtained using the optimum impedances is described in Fig.1. As can be seen in the figure, the maximum PAE is 84% while power gain and output power are 46.6 dBm and 14.1 dB, respectively. After determining the optimum impedances, the next design step is going to design matching networks and a biasing network. In the present study, matching and biasing networks are implemented using microstrip lines on a Megtron6 substrate supplied by Panasonic with the following parameters: thickness: 0.75 mm; conductor thickness: 0.35 μm; dielectric constant: 3.7; dielectric loss tangent: 0.002.

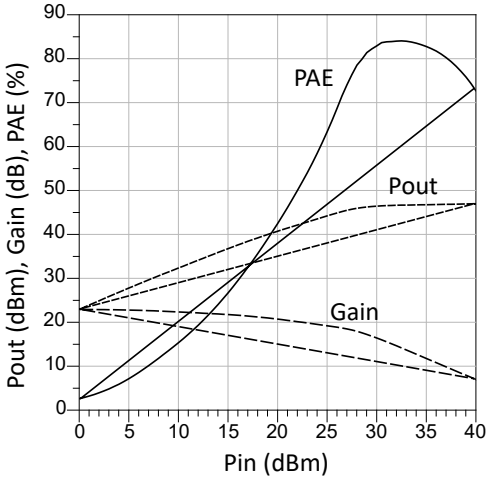

Fig. 1. SSPA response with optimum impedances. Here Pout and Gain denote output power and power gain while PAE means power-added efficiency.

2.1 Input matching network (IMN) design

Fig.2 shows the schematic of the IMN which is realized by using microstrip lines. Here, the IMN uses two open-stubs to realize the input impedances at fundamental frequency and second harmonic as shown in Table 1. The first open stub serves as a quarter-wave transmission line at the second harmonic while the second stub is adjusted at the fundamental frequency. Their physical dimensions including width (*W*) and length (*L*) are given as follows. All the transmission lines have equal width *W* of 1.6 mm while their lengths are: *L*(TL1) = 1 mm; *L*(TL2) = 10.5 mm; *L*(TL3) = 1 mm; *L*(TL4) = 17.8 mm; *L*(TL5) = 5 mm.

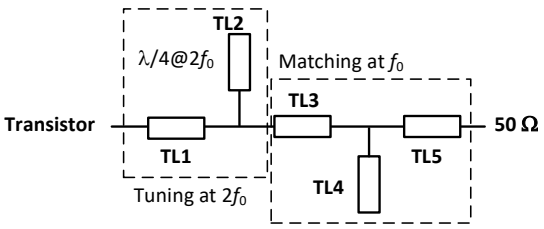

Fig. 2. Schematic of the IMN.

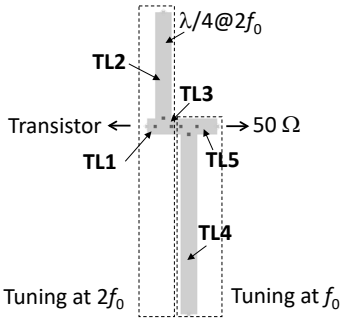

Fig. 3. EM model of the IMN.

Electro-magnetic (EM) simulation model of this IMN is illustrated in Fig. 3. Finally, the input impedances which are realized by the IMN are given in Fig.4 which shows frequency characteristic of the designed IMN on Smith chart.

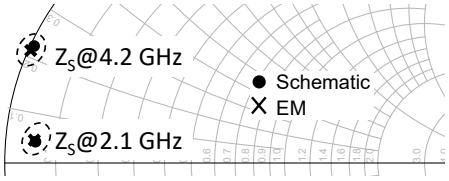

Fig. 4. Frequency characteristic of the IMN represented on the Smith chart.

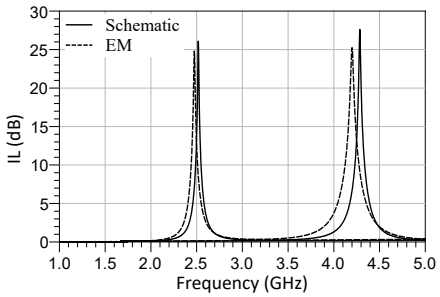

Fig. 5. Insertion loss of the IMN.

It can be clearly seen that both schematic and EM models of the IMN can realize the input impedances accurately regarding the values shown in Table 1. Finally, Fig.5 describes the loss of such an IMN for both schematic and EM models... The figure shows that the loss of both the schematic and EM model of the IMN is relatively low. At 2.1 GHz, they are 0.2 dB and 0.28 dB for the schematic and EM model, respectively. Here the insertion loss (*IL*) of the matching networks is evaluated by the following formula:

$$\mathrm{IL(dB)} = 10\log\left(\frac{1-|S_{11}|^2}{|S_{21}|^2}\right) \quad (6)$$

where S_{11} and S_{12} are the scattering parameters of the matching networks.

2.2. Output matching network (OMN) design

OMN is designed in a similar way as the IMN. However, three out impedances at the fundamental frequency, second harmonic and third harmonic have to be realized. In order to realize these impedances up to the third harmonic, three stubs are employed. The first and second stub function as the quarter-wave transmission lines for the third harmonic ($3f_0$) and second harmonic ($2f_0$), respectively while the third stub will be used to make an impedance matching at the fundamental frequency.

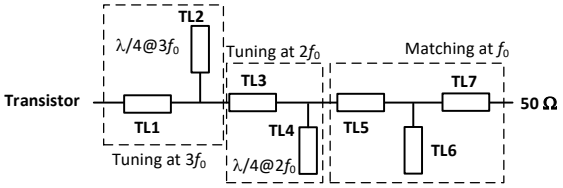

Fig. 6. Schematic of the OMN.

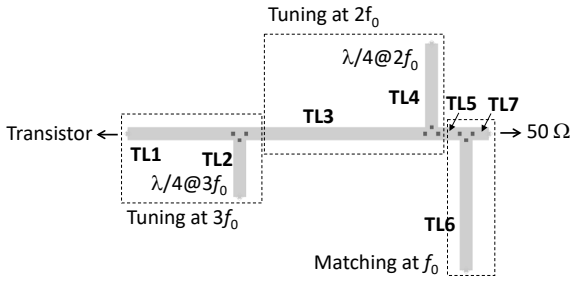

Fig. 7. EM model of the OMN.

Fig.6 shows the schematic of the OMN. Here, all the transmission lines have equal width *W* of 1.6 mm while their lengths are: *L*(TL1) = 13.37 mm; *L*(TL2) = 7 mm; *L*(TL3) = 22.46 mm; *L*(TL4) = 10.3 mm; *L*(TL5) = 2.66 mm; *L*(TL6) = 16 mm; *L*(TL7) = 2 mm. EM model of this schematic is given in Fig. 8 below. Fig.7 shows the EM model of the OMN. The output impedances which are realized by the OMN are given in Fig.8 below which shows frequency characteristic of the designed OMN on Smith chart.

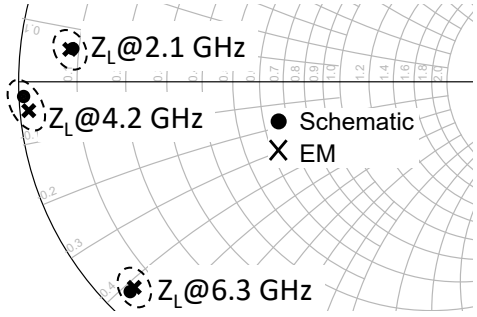

Fig. 8. Frequency characteristic of the OMN on the Smith chart.

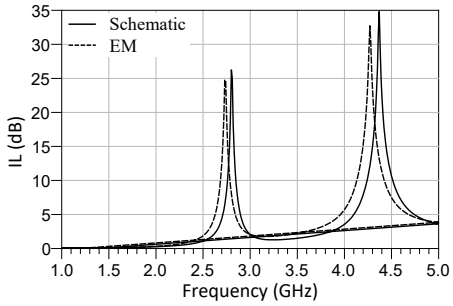

Fig. 9. Insertion loss of the OMN.

As can be clearly seen in the figure, both schematic and EM models of the OMN can realize the output impedances at fundamental frequency, second and third harmonics accurately regarding the ideal values shown in Table 1. Finally, Fig.9 shows the loss characteristic of such an OMN for both schematic and EM models. The loss of both the schematic and EM models of the OMN is acceptable. They are 0.36 dB and 0.44 dB for the schematic and EM model, respectively.

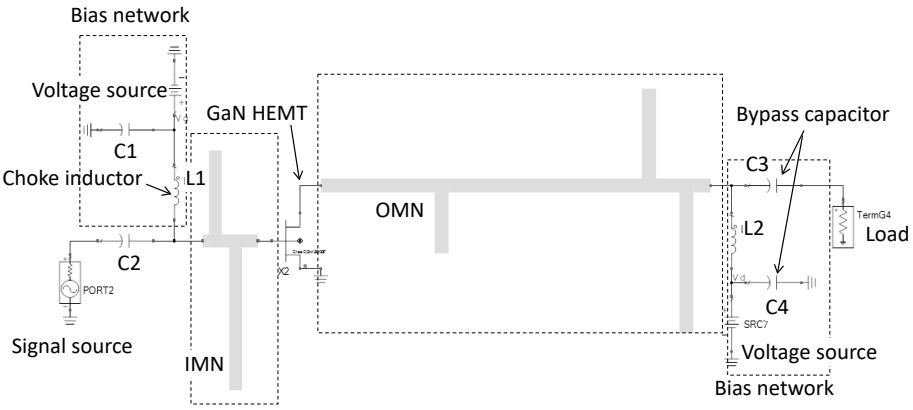

Fig. 10. Final ADS EM circuit for co-simulation

3. Simulated results

Fig.10 describes the final ADS schematic which is used to run a co-simulation to evaluate the circuit performances. Here, the IMN OMN uses the simulated EM models while the other components of the circuit such as the bias networks, bypass capacitors (C1, C2, C3, C4) use Murata models. The model series of the bypass capacitors are GRM1555C1H160JA01 with a value of 16 pF while the model series of the choke inductor (L1, L2) of the bias network is LQW18ANR16G00 with a value of 160 nH. It is worth noting that the self-resonant frequencies of the bypass capacitor and choke inductor are equal to the operating frequency of 2.1 GHz.

Finally, Fig.11 indicates the simulated results of the final schematic and EM circuits. The figure shows the simulated critical characteristics of the SSPA including output power, power gain and efficiency (PAE) for both the schematic and EM models at the operation frequency of 2.1 GHz. Their simulated performance is summarized in Table 2. From Fig.11 and Table 2, it can be concluded that the designed SSPA exhibits very good performance. It can deliver not only high power of 47.8 dBm saturated output power but also high efficiency of 73.2% PAE and high gain of 13.8 dB.

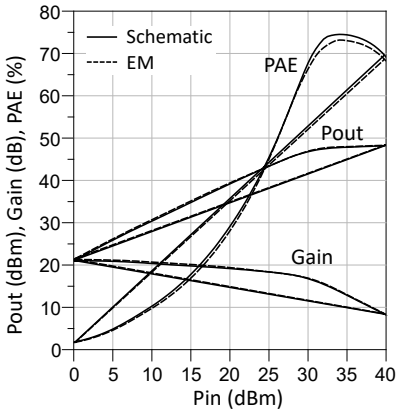

Fig. 11. Simulated results of the final circuit.

Table 2. Simulated schematic and EM performance summary

Model	P_{out} (dBm)	Gain (dB)	PAE (%)
Schematic	47.7	13.7	74.6
EM	47.8	13.8	73.2

Moreover, the deviation between the schematic and EM simulations is very small validating high accuracy of the design.

4. Conclusion

This study presents a design procedure for SSPAs to obtain high efficiency. The designed SSPA uses harmonic termination methods to improve efficiency. The simulated results show that the final designed SSPA operating at 2.1 GHz can deliver 47.8 dBm saturated output power with high efficiency of a 73.2% maximum PAE and a high gain of 13.8 dB. These promising results validate the accuracy of the design strategy.

Acknowledgments

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