Switched-Capacitor Nine-Level Inverter

Cấu Hình Nghịch Lưu Chuyển Tụ Điện 9 Bậc

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Abstract

This paper proposes a new configuration of the switched-capacitor multilevel inverter (SCMI). The proposed switched-capacitor nine-level inverter configuration based on switching the capacitors in series and in parallel through the semiconducting switches. The proposed topology does not use more power supplies to raise the output voltage level or the transformers to boost output voltage, moreover the proposed inverter of components are used less than the traditional inverter configuration, thereby reducing the cost and size of the system. To verify the circuit operation, PSIM simulation is performed for 9-level configuration. The experimental results are also shown with 9-level inverter configuration.

Keywords: Multilevel inverter, switched-capacitor, pulse-width modulation (PWM), boost voltage, reduced switch.

Tóm tắt

Bài báo này đề xuất một cấu hình mới của bộ nghịch lưu đa bậc chuyển tụ điện (SCMI). Cấu hình chuyển tụ điện 9 bậc đề xuất dựa trên việc chuyển đổi tụ điện mắc nối tiếp, song song với nguồn bằng các công tắc công suất bán dẫn. Cấu hình đề xuất không cần phải sử dụng nhiều nguồn ngõ vào để tăng số bậc điện áp ngõ ra hay các biến áp để tăng điện áp ngõ ra, ngoài ra cấu hình đề xuất cũng sử dụng số linh kiện ít hơn so với các cấu hình nghịch lưu truyền thống, do đó làm giảm chi phí và kích thước của hệ thống. Để kiểm chứng hoạt động của mạch, mô phỏng được thực hiện bằng phần mềm PSIM cho cấu hình nghịch lưu chuyển tụ điện 9 bậc đề xuất và thực nghiệm cũng được tiến hành với cấu hình này.

Từ khóa: Nghịch lưu đa bậc, chuyển tụ điện, phương pháp điều chế độ rộng xung, tăng điện áp, giảm công tắc bán dẫn trong mạch.

1. Introduction

The multilevel inverter (MI) is the one of the important components in the transformation of DC power source to AC power source. Today, under the development of clean energy sources: solar power, wind power, ... inverter has become an indispensable part. Along with the development of technology, inverter constantly improved in performance and quality. Multilevel inverter has the following advantages such as: improved output waveform quality, lower electronmagnetic-interface (EMI) and lower device stress.

In the field of motor control, the electricity storages, the electricity cars or the electricity distribution systems, ... the inverters are widely used. The multilevel inverter configurations are commonly used as the diode clamp configuration (NPC, Fig. 1(a)) [1], the flying capacitor (FC, Fig. 1(b)) [2], [3], The cascade H-bridge (CHB, Fig. 1(c)) [4], [5]. In the NPC, when the voltage level is greater than 3-level, the voltage spikes on the diodes will be different, moreover, the voltage balance of the DC sources become difficult when the level number is large. In the FC, the large number of capacitors are used which leads to gain costs and reduce the reliability of the system, and the control becomes difficult. The CHB is suitable for the medium and high power application due to its advantage for modularity and flexible expansion. Overall, these configurations use a large number of components (semiconductor switches, supplies, capacitors, diodes), which raises the cost of the inverter and the control becomes complicated.

To solve the problem in the traditional inverters, the switched-capacitor multilevel inverter (SCMI) was born and developed [6] - [11]. The SCMI uses charging and discharging characteristics of the capacitors to reduce the number of the sources in the circuit. In this configuration, the capacitor voltage can be balancing without having to use any additional circuit by using series and parallel conversion of the switches. In the parallel mode, the capacitors are charged directly by the power supply, while they release store energy during the series mode. By using switch capacitor structure, the system does not need

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more sources to increase the output voltage level or the transformer to boost the output voltage.

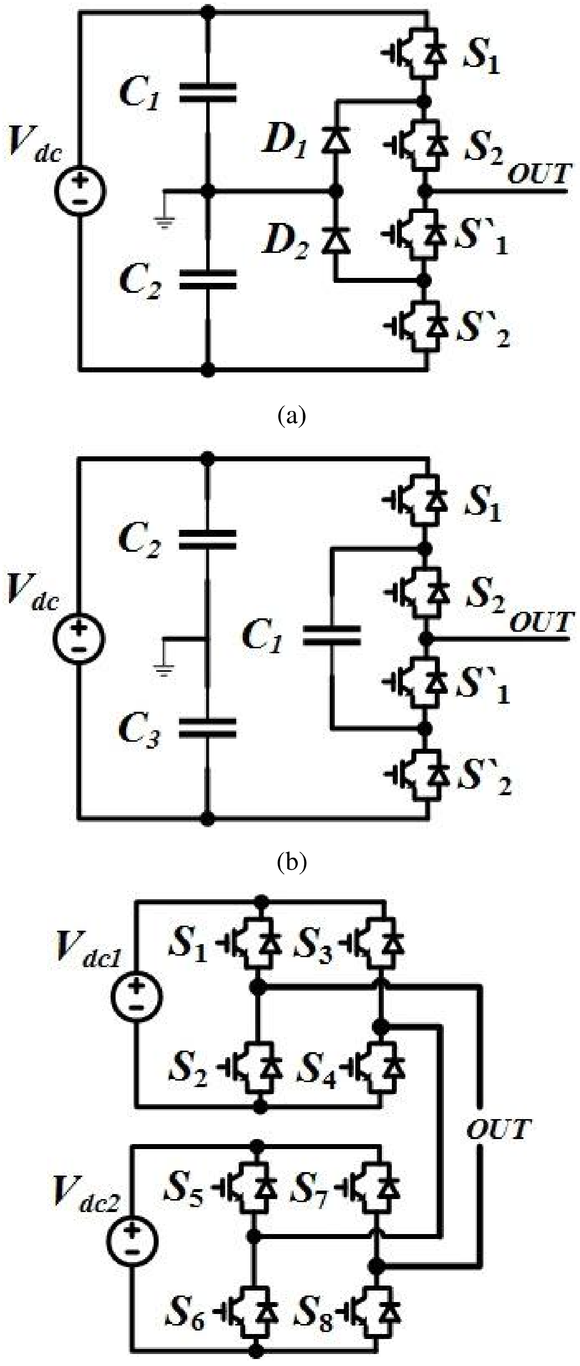

Fig. 1. The traditional inverter: (a) the diode clamp configuration (NPC), (b) the flying capacitor (FC), (c) The cascade H-bridge (CHB)

The article proposes a new SCMI which combine H-bridge circuit to generate the ladder voltage waveform at the output. In the proposed topology, the number of semiconductor switches in the circuit lower than the configuration has been investigated previous research. This paper presents the principles of operation of the the switched-capacitor 9-level inverter and verifying the operation of the proposed inverter through the simulation result by P.SIM 9.0 software. The study results are also demonstrated through experiments with physical model.

2. The proposed switched-capacitor nine-level inverter

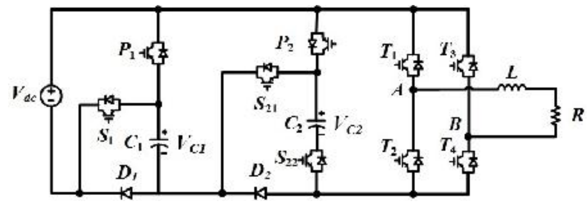

Fig. 2. The proposed switched-capacitor nine-level inverter.

2.1. The circuit description

The proposed SCMI was showed in Fig. 2 includes the switched-capacitor block with 5 semiconductor switches (S_1, S_{21}, S_{22}, P_1, P_2), 2 diodes (D_1, D_2), two capacitors (C_1, C_2) and one input source which connects parallel with the H-bridge circuit has four semiconductor switches (T_1, T_2, T_3, T_4).

In the operation circuit, the C_1 capacitor is charged when it connects in the parallel with input source through the P_1 switch and it is discharged when it connects in the series with the input source through the S_1 switch. Similarly, The C_2 capacitor is charged when it is in the parallel with the C_1 capacitor and the source through the P_2 switch and the anti-parallel diode of the S_{22} switch and it is discharged when it is in the series with the source and the C_1 capacitor through S_{21}, S_{22} switches.

2.2. The principle operation

Fig. 3 shows the operating status of the proposed inverter in a cycle includes: state 1 [Fig. 3(a)], a positive period has 4 states [state 2 to state 5, Fig. 3(b) to Fig. 3(e)] and a negative period has 4 states [state 6 to state 9, Fig. 3(f) to Fig. 3(i)].

During the positive period, the switches of the H-bridge circuit does not change the status, the T_1 and T_4 switches are in the ON state, the T_2 and T_3 switches are in the OFF state, the remaining components of the inverter circuit changes at each circuit operation state. The operation of the circuit is in state 1 and positive period is presented as follows:

+ State 1 [Fig. 3(a)]: At this state, the output voltage is V_{AB} = 0 V. The P_1, T_1 and T_3 switches are in the ON state,the S_1, T_2 and T_4 switches are in the

OFF state, the D_1 diode is forward-biased, the D_2 diode is reverse-biased, the C_1 capacitor is charged from the input source and $V_{C1} = V_{dc}$.

+ State 2 [Fig. 3(b)] The P_1 switch is in the ON state, the S_1 switch is in the OFF state, the D_1 and D_2 diodes are forward-biased, the C_1 capacitor is charged from the input source and $V_{C1} = V_{dc}$. At this state, the output voltage is $V_{AB} = V_{dc}$.

+ State 3 [Fig. 3(c)] The S_1 and P_2 switches are in the ON state, the P_1, S_{21} and S_{22} switches are in the OFF state, the D_1 diode is reverse-biased, the D_2 diode is forward-biased, the C_1 capacitor is discharge, the C_2 capacitor is charged form the input source and the C_1 voltage, $V_{C2} = V_{C1} + V_{dc} = 2V_{dc}$. In this state, the output voltage is $V_{AB} = V_{C1} + V_{dc} = 2V_{dc}$.

+ State 4 [Fig. 3(d)] The P1, S21 and S22 switches are in the ON state, the S1 and P2 switches are in the OFF state, the D1 diode is forward-biased, the D2 diode is reverse-biased, the C1 capacitor is charged from input source and VC1 = Vdc, the C2 capacitor is discharged. In this state, the output voltage is VAB = VC2 + Vdc = 3VDC.

+ State 5 [Fig. 3(e)] The S_1, S_{21} and S_{22} switches are in the ON state, the P_1 and P_2 switches are in the OFF state, the D_1 and D_2 diodes are reverse-biased, the C_1 and C_2 capacitors are discharged. In this state, the output voltage is $V_{AB} = V_{C1} + V_{C2} + V_{dc} = 4V_{dc}$.

In the negative period, the status of the switches in the H-bridge circuit is opposite with the positive period, the T2 and T3 switches are in the ON state, the T1 and T4 switches are in the OFF state, the remaining components the inverter circuit change similar to the positive period in each circuit operation state. All operational state of the semiconductor switches and diodes in the proposed topology are shown in Table 1.

Table 1. The main components of fresh cassava

No.	The switches and diodes in the ON state	Output Voltage
1	S_1, S_{21}, S_{22}, T_1, T_4	$4V_{dc}$
2	P_1, S_{21}, S_{22}, T_1, T_4, D_1	$3V_{dc}$
3	S_1, P_2, T_1, T_4, D_2	$2V_{dc}$
4	P_1, T_1, T_4, D_1, D_2	V_{dc}
5	P_1, T_1, T_3, D_1	0 V
6	P_1, T_2, T_3, D_1, D_2	$-V_{dc}$
7	S_1, P_2, T_1, T_3, D_2	$-2V_{dc}$
8	P_1, S_{21}, S_{22}, T_2, T_3, D_1	$-3V_{dc}$
9	S_1, S_{21}, S_{22}, T_2, T_3	$-4V_{dc}$

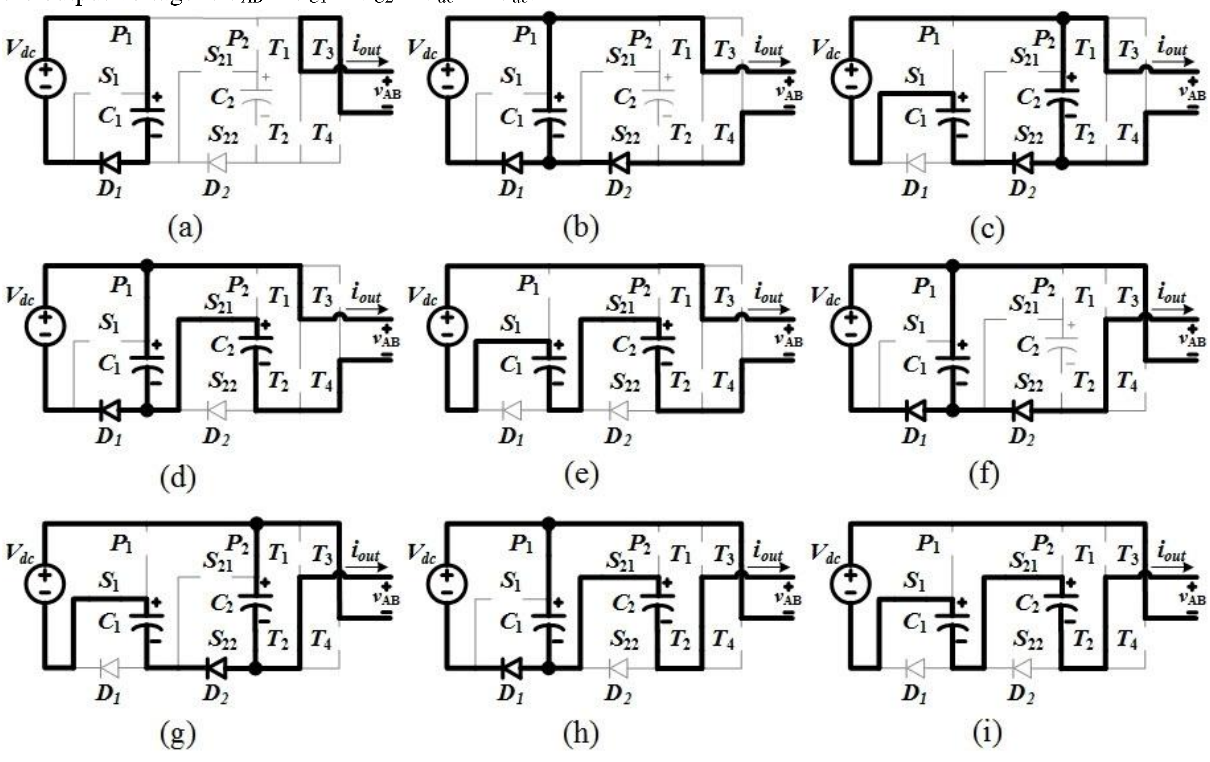

Fig. 3. The operation states of proposed inverter. (a) state 1; (b) state 2; (c) state 3; (d) state 4; (e) state 5; (f) state 6; (g) state 7; (h) state 8; (i) state 9.

3. The simulation and experiment results

To verify the operation of the proposed switched-capacitor nine-level inverter, the simulations and experiments were conducted according to the schematic in Fig. 2 for 2 instance:

+ Case 1: The resitive load (R = 80 Ω).

+ Case 2: The passive load (R = 80 Ω, L=30 mH).

The input voltage V_{dc} = 48 V, the capacitance of the capacitors $C_1 = C_2$ = 2200 µF.

3.1. The simulation result

3.1.1. The resitive load (R = 80 Ω)

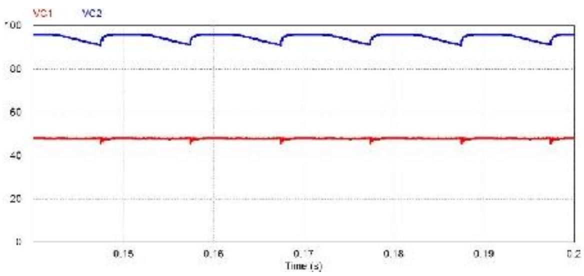

Fig. 4. The C_1 and C_2 voltage waveform of the capacitors (V_{C1}, V_{C2}).

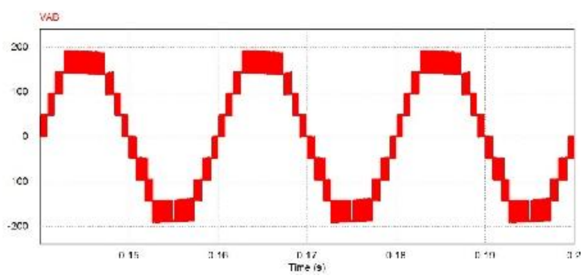

Fig. 5. The output voltage waveform V_{AB} *(R = 80 Ω)*.

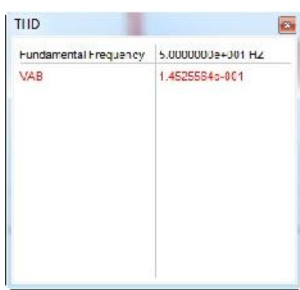

Fig. 6. The total harmonic distortion (THD) of the output waveform (R = 80 Ω).

The Fig. 4 is a C_1 and C_2 voltage waveform. The maximum and minimum values of the C_1 voltage are 48 V and 45.5 V, respectively. The maximum and minimum of the C_2 voltage are 96 V and 91.1 V, respectively. The Fig. 5 is the output voltage waveform of the proposed SCMI with the total harmonic distortion is 14.52% as in the Fig. 6.

3.1.2. The passive load (R = 80 Ω, L=30 mH).

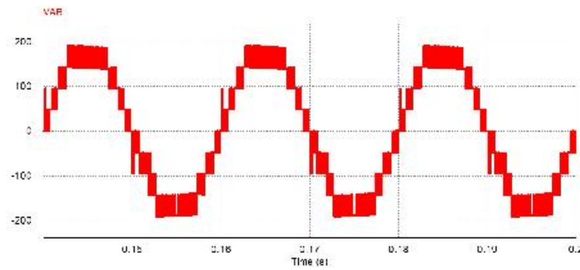

Fig. 7. The output voltage waveform V_{AB} (R = 80 Ω, L = 30 mH)

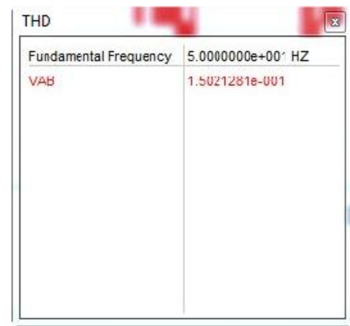

Fig. 8. The total harmonic distortion (THD) of the output waveform (R = 80 Ω, L = 30 mH).

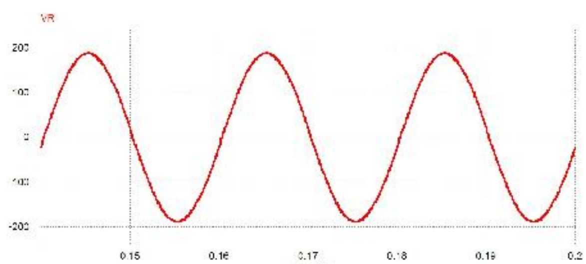

Fig. 9. The R voltage waveform V_{AB} (R = 80 Ω, L = 30 mH)

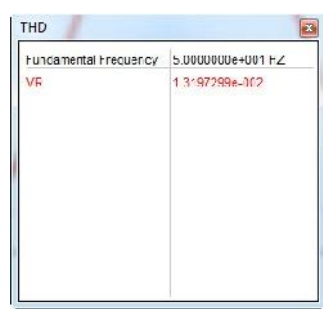

Fig. 10. The total harmonic distortion (THD) of the R voltage waveform *(R = 80* Ω, L = 30 mH).

The voltage waveform of the capacitors get from the simulation, the passive load is similar with the resistive in the Fig 4.

The Fig. 7 shows the output voltage waveform of the proposed SCMI with the total harmonic distortion is 15.02% as in the Fig. 8. This THD value of the passive load is bigger than the resitive load. However, the R voltage waveform shows in the Fig. 9 has the THD value is small (THD = 1.32 %, Fig. 10).

3.2. The experiment results

3.1.1. The resitive load (R = 80 Ω)

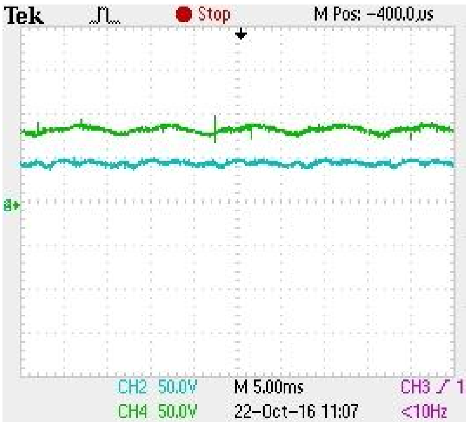

Fig. 11. The C_1 and C_2 voltage waveform of the capacitors (V_{C1}, V_{C2}).

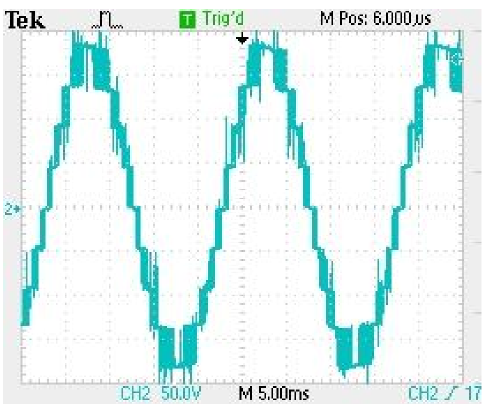

Fig. 12. The output voltage waveform V_{AB} (R = 80Ω).

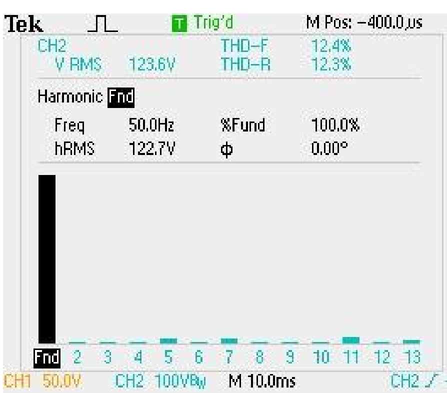

Fig. 13. The total harmonic distortion (THD) of the output waveform (R = 80 Ω).

The Fig. 11 is a C_1 and C_2 voltage waveform. The maximum and minimum values of the C_1 voltage are 47 V and 43.5 V, respectively. The maximum and minimum of the C_2 voltage are 90 V and 85.5 V, respectively. The Fig. 12 is the output voltage waveform of the proposed SCMI with the total harmonic distortion is 12.4 % as in the Fig. 13.

3.1.2. The passive load (R = 80 Ω, L=30 mH).

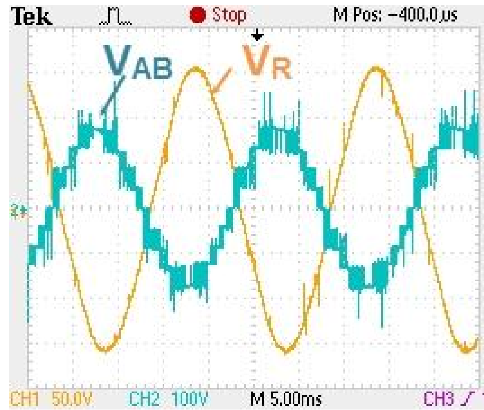

Fig. 14. The output voltage waveform (V_{AB}) and the R voltage waveform (V_R) *(R = 80* Ω,L = 30 mH).

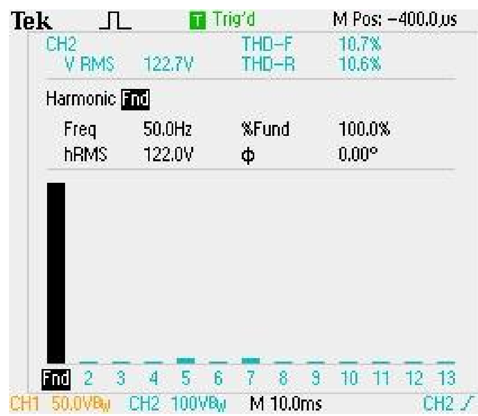

Fig. 15. The total harmonic distortion (THD) of the output waveform *(R = 80* Ω*, L = 30 mH).*

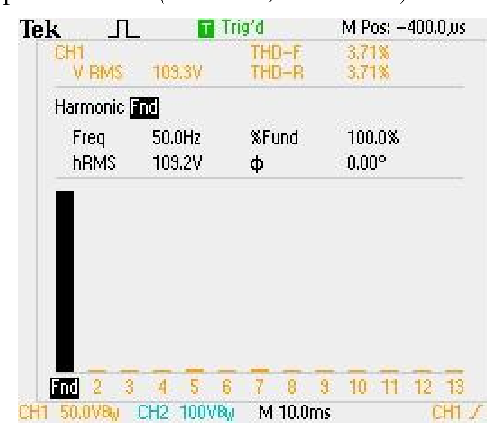

Fig. 16. The total harmonic distortion (THD) of the R voltage waveform (R = 80 Ω, L = 30 mH).

The voltage waveform of the capacitors get from the experiment, the passive load is similar with the resistive in the Fig 11.

The Fig. 14 shows the output voltage waveform (V_{AB}) and the R voltage waveform (V_R) of the proposed SCMI with the total harmonic distortion of the output voltage waveform is 10.7 % as in the Fig. 15. This THD value of the passive load is bigger than the resitive load. However, the R voltage waveform has the THD value is small (THD = 3,71 %, Fig. 16).

After the performing of the simulation and experiment, the results of simulations and the experiments is approximately.

4. Conclusion

This paper proposes a new switched-capacitor multilevel inverter. This paper presents the operation theory of the switched-capacitor nine-level inverter. Based on theory, the proposed inverter was simulated on the software PSIM 9.0 and the circuit operability is also proven by the fact pattern. Overall, the proposed SCMI has the number of components significantly reduced compared with conventional inverter circuits thus saving cost and reducing complexity in control.

References

[1] A. Nabae, I. Takahashi, H. Akagi, A new neutral-point-clamped PWM inverter, IEEE Trans. Ind. Appl, IA-17, 5, (1981) 518–523.

[2] X. Kou, K. A. Corzine, Y. L. Familiant, A unique fault-tolerant design for flying capacitor multilevel inverter, IEEE Trans. Power Electron, 19, 4, (2004) 979–987.

[3] M. Khazraei, H. Sepahvand, K. A. Corzine, M. Ferdowsi, Active capacitor voltage balancing in single-phase flying-capacitor multilevel power converters, IEEE Trans. Ind. Electron, 59, 2, (2012) 769–778.

[4] M. Malinowski, K. Gopakumar, J. Rodriguez, M. A. Pérez, A survey on cascaded multilevel inverters, IEEE Trans. Ind. Electron, 57, 7, (2010) 2197–2206.

[5] A. Ghazanfari, H. Mokhtari, and M. Firouzi, Simple voltage balancing approach for CHB multilevel inverter considering low harmonic content based on a hybrid optimal modulation strategy, IEEE Trans. Power Del, 27, 4, (2012) 2150–2158.

[6] Y. Hinago, H. Koizumi, A switched-capacitor inverter using series/ parallel conversion, IEEE Int. Symp. Circuits Syst, (2010) 3188–3191.

[7] Y. Hinago, H. Koizumi, A Switched-Capacitor Inverter Using Series/Parallel Conversion with Inductive Load, IEEE Trans. Ind. Electron, 59, 2, (2012) 878-887.

[8] M. B. Kalashani, M. Farsadi; A new switched-capacitors boost inverter for renewable energy sources and POD control modulation; Electrical Engineering (ICEE); Iran; 2014; 636 - 641.

[9] E. Babaei, S. S. Gowgani, Hybrid Multilevel Inverter Using Switched Capacitor Units, IEEE Trans. Ind. Electron, 61, 9, (2014) 4614-4621.

[10] A. Tsunoda, Y. Hinago, H. Koizumi, Level- and Phase-Shifted PWM for Seven-Level Switched-Capacitor Inverter Using Series/Parallel Conversion, IEEE Trans. Ind. Electron, 61, 8, (2014) 4011-4021.

[11] O. C. Mak, A. Ioinovici, Switched-capacitor inverter with high power density and enhanced regulation capability, IEEE Trans. Circuits Syst. I, Fundam. Theory Appl, 45, 4, (1998) 336–347.