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A Simple Space Vector Modulation to Eliminate Zero Sequence Voltage with Balanced Neutral Point Voltage for a New Five-Level Voltage Source Inverter

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Abstract

In the paper, a new three-phase five-level voltage source inverter (VSI) topology is developed by utilizing six three-level F-type legs. The proposed topology reduces the number of power electronic components while operating with a single DC source, offering advantages over conventional three-phase five-level VSI topologies. The operating principles are analyzed theoretically, and a simplified space vector modulation (SVM) method is introduced to control the proposed topology. In the proposed SVM approach, 19 voltage vectors are strategically selected for modulation to regulate the inverter while effectively eliminating the zero-sequence voltage (ZSV) component. Furthermore, balanced capacitor voltages are achieved by leveraging the opposite effects of redundant switching states on the neutral-point voltage. Consequently, the proposed SVM method enables simultaneous capacitor voltage balancing and elimination of the zero-sequence voltage (ZSV) component without requiring the adjustment of a balancing control factor. Simulation results are presented to validate the effectiveness of the proposed VSI topology and its modulation strategy.

Keywords: Balanced capacitor voltages, five-level voltage source inverter, space vector modulation, zero-sequence voltage component.

1. Introduction

Multilevel inverters provide several notable advantages over conventional two-level inverters, including reduced voltage stress of power devices, lower total harmonic distortion (THD), reduced *dv/dt*, decreased filter size, and diminished electromagnetic interference (EMI) [1]. These superior characteristics have facilitated the extensive implementation of multi-level inverters across a range of industrial applications, such as motor drives, power conditioning systems, photovoltaic energy conversion, electric vehicles, high-voltage direct current (HVDC) transmission, and wind energy generation systems [2-5]. Numerous multilevel inverter (MLI) topologies have been extensively documented in the literature, with the most prominent configurations including the neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) inverters [6-8]. The NPC topology necessitates the use of multiple clamping diodes, while the FC and CHB topologies require floating capacitors and isolated direct current (DC) sources, respectively, as the number of phase voltage levels increases. Furthermore, both the FC and NPC topologies are susceptible to capacitor voltage imbalance issues, which can compromise system stability and performance. Although the CHB inverter offers performance benefits, its reliance on multiple isolated DC sources contributes to increased system complexity and bulkiness.

Numerous enhanced three-phase five-level inverter topologies with a reduced number of power electronic components have been proposed in [9-14]. A five-level NPC/H-bridge topology was introduced in [9,10] by combining the Neutral-Point-Clamped (NPC) and H-bridge configurations. While this topology reduces the number of isolated DC sources compared to the five-level Cascaded H-Bridge (CHB) topology, it still necessitates three isolated DC sources. To further minimize the number of isolated DC sources, a three-phase five-level inverter topology was proposed in [11, 12], utilizing 24 active switches, two capacitors, and 12 diodes while requiring only a single DC source. In an effort to eliminate diode usage, the authors in [13] introduced a five-level topology that employs two-level inverters in series with a capacitor-fed H-Bridge cell. However, this topology presents a complex control strategy due to the necessity of maintaining voltage balance across three capacitors. In [14], a three-phase five-level voltage source inverter (VSI) topology with 18 active switches was proposed, eliminating the requirement for balanced capacitor voltages. Nevertheless, this topology still requires two isolated DC sources, leading to increased system size and cost.

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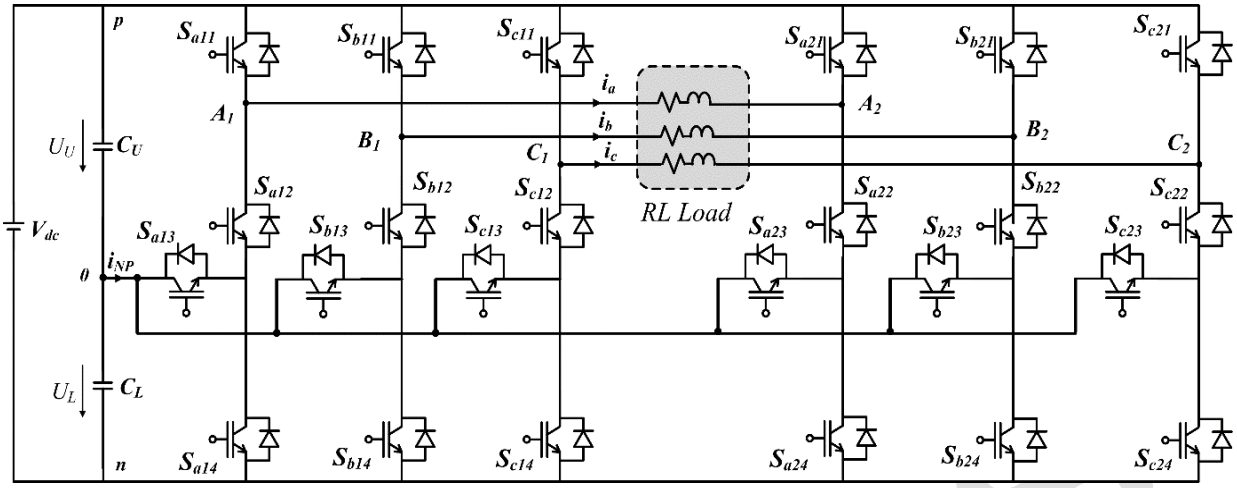

Fig. 1. The proposed three-phase five-level VSI topology

To reduce the number of power electronic components while utilizing only a single DC source, this paper presents a novel three-phase five-level voltage VSI topology based on six three-level F-type legs. The operating principle of the proposed topology is analyzed theoretically, including its voltage levels, and a simplified space vector modulation (SVM) technique is developed for its control. In the proposed SVM approach, 19 voltage vectors are systematically selected for modulation to effectively eliminate the zero-sequence voltage (ZSV) component, while the counteracting effects of redundant switching states on the neutral-point voltage are utilized to achieve balanced capacitor voltages. Therefore, the proposed SVM method effectively balances capacitor voltages and eliminates the ZSV component without requiring the balancing control factor adjustment process used in [11]. To validate the effectiveness of the proposed VSI topology and its modulation strategy, simulation results are provided.

2. Proposed Five-Level Voltage Source Inverter Topology

2.1. Topology

The configuration of the proposed five-level VSI with a single DC source is depicted in Fig. 1, along with a three-phase open-end load. This topology consists of two three-phase three-level F-type VSIs, which are connected to the terminals (A_1, B_1, C_1) and (A_2, B_2, C_2) of the open-end load. The two inverters within the proposed five-level VSI are designated as Inverter 1 and Inverter 2. The proposed inverter is composed of 24 IGBTs and two capacitors for the common DC-link stage. As illustrated in Fig. 1, V_{dc} represents the DC-link voltage, while "0" denotes the neutral point of the DC bus; C_1 and C_2 are the upper and lower DC-link capacitors, respectively, whereas "*p*" and "*n*" indicate the positive and negative DC-link bus.

2.2. Switching States

The proposed topology consists of six three-level F-type legs, with each leg comprising four insulated-gate bipolar transistors (IGBTs) arranged in two complementary switch pairs: S_{x1} and S_{x2}, as well as S_{x3} and S_{x4}, where x corresponds to a_1, b_1, c_1, a_2, b_2, c_2. Each leg operates with three distinct switching states, as detailed in Table 1, where the ON and OFF states are represented by "1" and "0," respectively. The phase voltages of the proposed topology can be determined using the following equation:

$$\begin{aligned} V_a &= V_{A_1O} - V_{A_2O} \\ V_b &= V_{B_1O} - V_{B_2O} \\ V_c &= V_{C_1O} - V_{C_2O} \end{aligned} \tag{1}$$

where V_{A_1O}, V_{B_1O}, and V_{C_1O} represent the pole voltages of Inverter 1, while V_{A_2O}, V_{B_2O}, and V_{B_2O} represent the pole voltages of the Inverter 2.

Table 1. Switching states of a three-level F-type leg

Switching State	**Voltage leg U_{XO} (X= A_1, B_1, C_1, A_2, B_2, C_2)**	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P	$V_{dc}/2$	1	0	1	0
O	0	0	1	1	0
N	$-V_{dc}/2$	0	1	0	1

As a result, each phase of the proposed inverter can produce nine distinct switching states, corresponding to five distinct output voltage levels (V_{dc}, 0.5 V_{dc}, 0, -0.5 V_{dc}, - V_{dc}), as summarized in Table 2. Fig. 2 depicts the generation of the V_{dc} voltage level in phase *a*.

Table 2. Switching states of the phase *a* of the proposed topology

S_{a11}	S_{a13}	S_{a21}	S_{a23}	V_a
1	1	0	0	V_{dc}
1	1	0	1	$V_{dc}/2$
0	1	0	0	$V_{dc}/2$
0	1	0	1	0
0	0	0	0	0
1	1	1	1	0
0	1	1	1	$-V_{dc}/2$
0	0	0	1	$-V_{dc}/2$
0	0	1	1	$-V_{dc}$

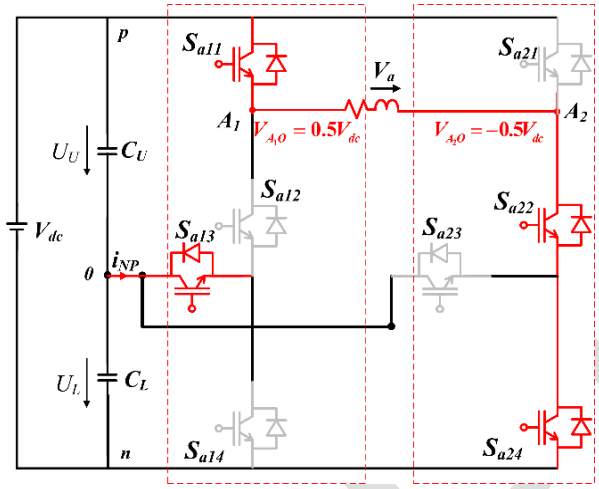

Fig. 2. The generation of the V_{dc} voltage level in phase *a*

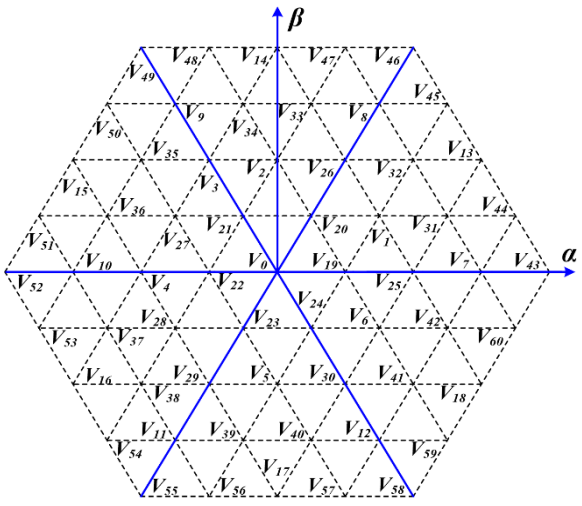

Fig. 3. Space vector diagram of the proposed topology

The proposed five-level VSI is capable of generating 729 distinct switching state combinations. Each switching state combination corresponds to a specific voltage vector, which is mapped onto the (α-β) plane using the Clarke transformation, as expressed by the following equation:

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \quad (2)$$

Fig. 3 shows the total of 61 voltage vectors of the proposed topology.

2.3. Zero-Sequence Voltage Component

Let V_{zsv} denote the ZSV component of the proposed topology, which is mathematically expressed as follows [11]:

$$V_{ZSV} = V_{CMV1} - V_{CMV2} \quad (3)$$

where V_{CMV1} and V_{CMV2} represent the common-mode voltages of the Inverter 1 and the Inverter 2, respectively. These voltages are defined as follows:

$$V_{CMV1} = (V_{A_1O} + V_{B_1O} + V_{C_1O})/3 \quad (4)$$

$$V_{CMV2} = (V_{A_2O} + V_{B_2O} + V_{C_2O})/3 \quad (5)$$

The configuration of the proposed five-level topology, which is powered by a single DC source, inherently generates the ZSV component V_{ZSV} . This component, in turn, induces a zero-sequence current (ZSC) i_{ZSC}, defined as:

$$i_{ZSC} = \frac{i_a + i_b + i_c}{3} \quad (6)$$

where i_a, i_b, and i_c represent the output currents of phases *a*, *b*, and *c*, respectively. The presence of ZSC contributes to additional power losses and introduces distortion in the output currents, as discussed in [3]. Therefore, the elimination of the ZSV component is essential for improving the overall performance and efficiency of the system.

2.4. Comparison

A comparative analysis of the proposed five-level topology and alternative five-level VSI topologies is presented in Table 3.

This analysis considers key parameters, including the number of switching devices, clamping diodes, electrolytic flying capacitors, and DC sources. The primary findings from this comparison are summarized.

The proposed five-level voltage source inverter (5L-VSI) retains the same number of power switches as the five-level neutral-point-clamped (5L-NPC) topology [2] and the five-level flying capacitor (5L-FC) topology [6]. However, it eliminates the requirement for clamping diodes, thereby simplifying the assembly and maintenance process. Additionally, the 5L-NPC topology necessitates a more complex control strategy to maintain voltage balancing across its four DC-link capacitors. Moreover, compared to the 5L-FC topology, the proposed design reduces the number of flying capacitors by 83.3% and exhibits lower control complexity.

Table 3. Comparison between the proposed topology and conventional five-level VSI topologies

Topology	Number of switches	Number of capacitors	Number of diodes	Number of DC sources
5 level-NPC [2]	24	4	12	1
5 level -FC [6]	24	12	0	1
5 level - CHB [7]	24	0	0	6
5 level - HNPC [8]	24	6	12	3
5 level - topology [11]	24	2	12	1
5 level - topology [13]	24	3	0	1
5 level - topology [14]	18	0	0	2
The proposed 5 level - topology	24	2	0	1

In comparison with the 5L-CHB topology [7] and the five-level topology introduced in [14], the proposed topology operates without the need for an isolated DC source and eliminates the phase-shifting transformer. As a result, it achieves a more compact design with lower implementation costs relative to these existing topologies.

Furthermore, compared to the 5L-HNPC topology presented in [8], the proposed 5L-VSI topology eliminates the necessity for both clamping diodes and isolated DC sources. Consequently, this reduction in components leads to a significant decrease in both system size and overall cost.

Relative to the five-level topology outlined in [11], the proposed topology maintains an equivalent number of power switches. However, by eliminating clamping diodes, it reduces system complexity and enhances the ease of assembly and maintenance.

Additionally, compared to the five-level (5L) topology described in [13], the proposed 5L-VSI requires 33.3% fewer capacitors. Since capacitors are generally more prone to failure than power semiconductor devices, minimizing their quantity enhances the reliability of the proposed 5L-VSI. Furthermore, the proposed topology simplifies the control mechanism required for maintaining balanced capacitor voltages in contrast to the 5L topology in [13].

Based on this comparative analysis, the advantages of the proposed five-level topology can be summarized as follows: it requires fewer power electronic components than other five-level VSI topologies powered by a single DC source, leading to improvements in cost-effectiveness, reliability, and system efficiency.

3. Simple Space Vector Modulation Method for the Proposed Topology

In addition to the requirement of eliminating the ZSV component, ensuring the balance of capacitor voltages in the proposed topology is essential. Voltage imbalances in the capacitors can degrade the quality of the output voltage and increase the voltage stress on switching devices, potentially leading to their failure [12,13]. To address these issues, a SVM method has been proposed. However, its implementation becomes increasingly complex due to the requirement of adjusting the balancing control factor. To overcome these limitations, a simplified SVM method is presented in the following section. The proposed method effectively balances capacitor voltages and eliminates the ZSV component without the need for parameter adjustment.

3.1. Selected Voltage Vectors

According to (3), among the 61 voltage vectors in the proposed topology, 19 voltage vectors exhibit a zero ZSV component, as illustrated in Fig. 4. Consequently, these 19 voltage vectors can be selected to eliminate ZSV in the proposed five-level VSI. These voltage vectors comprise one zero vector and 18 active vectors, which are categorized based on their amplitude as follows:

- Small voltage vectors (SV): Vectors $V_1 - V_6$
- Medium voltage vectors (MV): Vectors $V_7 - V_{12}$
- Large voltage vectors (LV): Vectors $V_{13} - V_{18}$

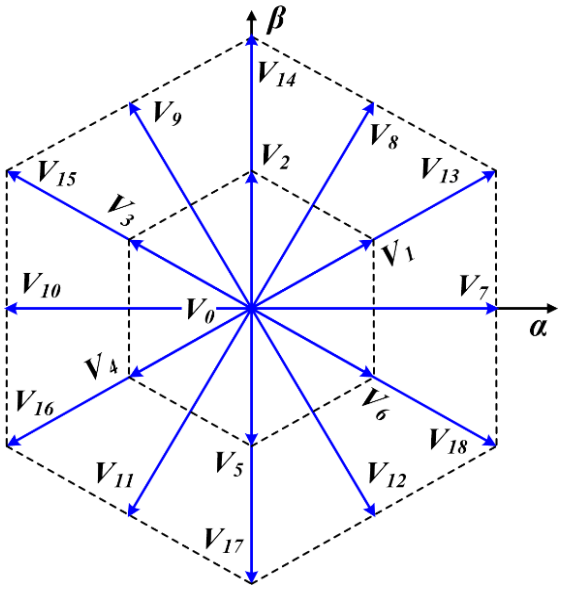

Fig. 4. Selected voltage vectors for the proposed SVM method

The zero-voltage vector has nine possible switching combinations. Each small voltage vector corresponds to 12 switching states, each medium voltage vector has four switching states, and each large voltage vector has three switching states [4]. The switching states of the zero-voltage vector, along with two of the three switching states for each large voltage vector, do not influence the neutral-point voltage. However, the medium voltage vectors contribute to the deviation of the two capacitor voltages. Additionally, each small voltage vector has two pairs of switching combinations that exert opposing effects on the neutral-point potential. By leveraging these switching states, it is possible to regulate and balance the neutral-point voltage.

Based on these two principles, the 19 voltage vectors depicted in Fig. 4 are selected for modulation in the proposed five-level VSI to achieve simultaneous capacitor voltage balancing and elimination of the ZSV component.

3.2. Duration Times for Voltage Vectors

The space voltage vector diagram of the proposed SVM technique is partitioned into six distinct sectors. The first sector spans the angular range from $-\pi/6$ to $\pi/6$, with each subsequent sector being incrementally shifted counterclockwise by an angle of $\pi/3$, as illustrated in Fig. 4. In the proposed SVM approach, each sector is further subdivided into four smaller regions, designated as the Region 1, the Region 2, the Region 3, and the Region 4, as depicted in Fig. 5. The synthesis of the reference output voltage vector is achieved by utilizing the three nearest voltage vectors. For instance, when the reference output voltage vector resides in Region 1 of Sector 1, as shown in Fig. 5, the voltage vectors V_0, V_1, and V_6 are selected to construct the reference output voltage vector. The corresponding duration times are computed based on the following constraints:

$$\begin{aligned} T_s V_{ref} &= T_{V0} V_0 + T_{V1} V_1 + T_{V6} V_6 \\ T_s &= T_{V0} + T_{V1} + T_{V6} \end{aligned} \tag{5}$$

where T_{V1}, T_{V6}, and T_{V0} represent the duration times associated with the vectors V_1, V_6, and V_0, respectively. Additionally, T_s is the sampling period.

Consequently, the corresponding duration times are determined as follows:

$$\begin{aligned} T_{V1} &= 2 * \frac{V_{ref}}{V_{dc}} \sin(\frac{\pi}{6} + \theta) = 2 * m \sin(\frac{\pi}{6} + \theta) \\ T_{V6} &= 2 * \frac{V_{ref}}{V_{dc}} \sin(\frac{\pi}{6} - \theta) = 2 * m \sin(\frac{\pi}{6} - \theta) \\ T_{V0} &= T_s - T_{V1} - T_{V6} \end{aligned} \tag{6}$$

where $m = V_{ref}/V_{dc}$ is the modulation index.

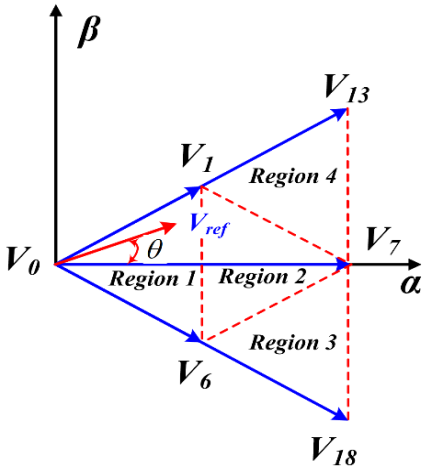

Fig. 5. Reference output voltage vector synthesis in the proposed SVM method

3.3. Switching Patterns for Balancing Capacitor Voltages

After determining the three voltage vectors and their corresponding execution times, the appropriate switching sequence is formulated to maintain neutral-point voltage balance. The neutral-point voltage is then defined as follows:

$$U_{NP} = U_U - U_L \tag{7}$$

The influence of switching states on the neutral-point voltage is illustrated in Fig. 6. Specifically, the switching states corresponding to the zero-voltage vector, along with two of the three switching states associated with each large voltage vector, do not impact the neutral-point voltage. This phenomenon arises because the phase currents are directly connected to either the positive or negative DC bus, while the neutral point (O) remains electrically isolated, as depicted in Fig. 6(a) and Fig. 6(b) [15]. Each small voltage vector corresponds to twelve distinct switching states. Among these, two sets of switching combinations exert opposing effects on the neutral-point potential. For instance, the small voltage vector V_1 comprises two pairs of switching combinations: one consisting of POO-OOP and ONN-NNO, and the other comprising PPO-OPP and OON-NOO. In this configuration, POO-OOP and PPO-OPP correspond to the P-type switching state, whereas ONN-NNO and OON-NOO correspond to the N-type switching state.

Fig. 6 (c) illustrates the inverter operation under the P-type switching state POO-OOP of voltage vector V_1, where the phase currents are connected to the positive DC bus and the neutral point O, leading to neutral current i_{NP} flow into the neutral point. Consequently, the voltage of the lower capacitor increases while that of the upper capacitor decreases [15], resulting in a reduction of the neutral-point voltage.

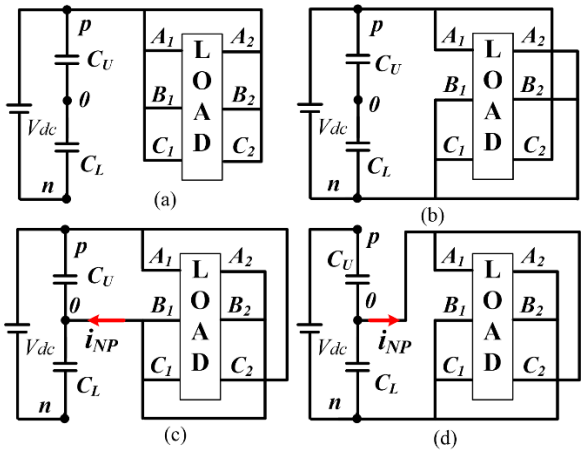

Fig. 6. Effect of switching states on the neutral-point voltage. (a) Zero vector V_0 (PPP-PPP). (b) Large vector V_{13} (PNN-NNP). (c) P-type switching state of small vector V_1 (POO-OOP). (d) N-type switching state of small vector V_1 (ONN-NNO)

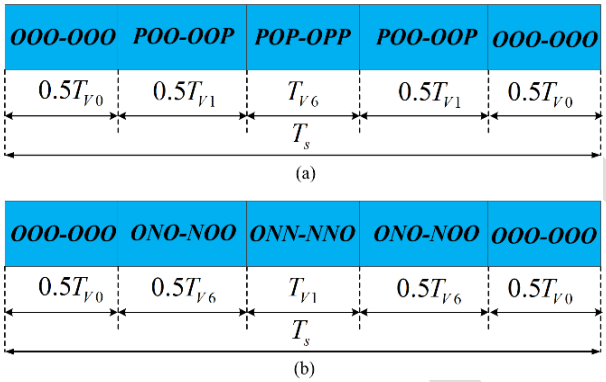

Fig. 7. The switching patterns utilized to achieve a balanced neutral-point voltage in the proposed SVM method with (a) $U_U > U_L$, (b) $U_U < U_L$

Conversely, when the inverter operates with the N-type switching state ONN-NNO of voltage vector V_1 , the phase currents are connected to the negative DC bus and the neutral point O, as shown in Fig. 6(d). This configuration causes an increase in the neutral-point voltage. By selecting and controlling appropriately these switching states, it is possible to regulate and maintain the balance of the neutral-point voltage.

Fig. 7 illustrates the switching pattern of the proposed SVM method designed to balance the capacitor voltages. When the voltage of the lower capacitor exceeds that of the upper capacitor, N-type switching states of the small voltage vectors are employed to regulate the neutral-point voltage. Conversely, if the upper capacitor voltage surpasses the lower capacitor voltage, P-type switching states of the small voltage vectors are utilized to maintain neutral-point voltage control.

4. Simulation Results

The simulations were conducted using PSIM 9.0 software to evaluate the effectiveness of the proposed SVM method for the newly developed three-phase five-level VSI. The simulation parameters were set as follows: the DC-link voltage V_{dc} was 400 V; the capacitance of the two capacitors was C_1=C_2=1500 uF; the R-L load consisted of a resistance R of 13 Ω and an inductance L of 15 mH; the output frequency was 50 Hz; and the sampling period was 100 µs.

Fig. 8 presents the output phase voltage, output currents, capacitor voltages, neutral-point voltage, and ZSV component of the proposed topology at a modulation index of m = 0.3. As illustrated in Fig. 8(a), the output phase voltage exhibits a three-step waveform with a THD of 105%. The three-phase output currents maintain a sinusoidal shape with a THD of 3.2%, as depicted in Fig. 8(b). Additionally, the capacitor voltages are effectively regulated at 200 V, and the ZSV component is successfully eliminated, as shown in Fig. 8(c) and Fig. 8(e).

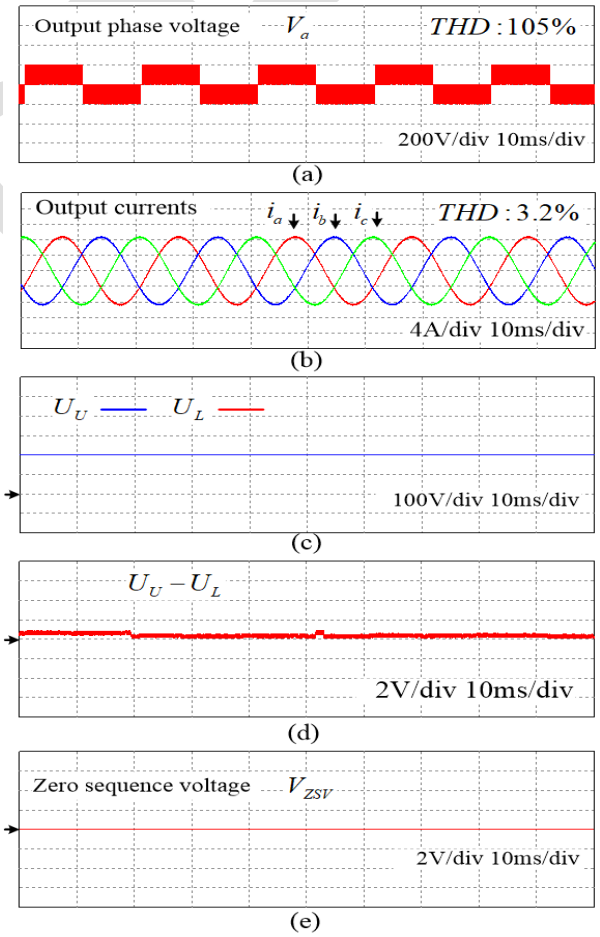

Fig. 8. Simulation results of the proposed SVM method at m = 0.3: (a), output phase voltage V_a (b), output currents i_a, i_b, i_c (c), capacitor voltages U_U, U_L, (d) neutral-point voltage U_U-U_L, and (e), ZSV component V_{ZSV}

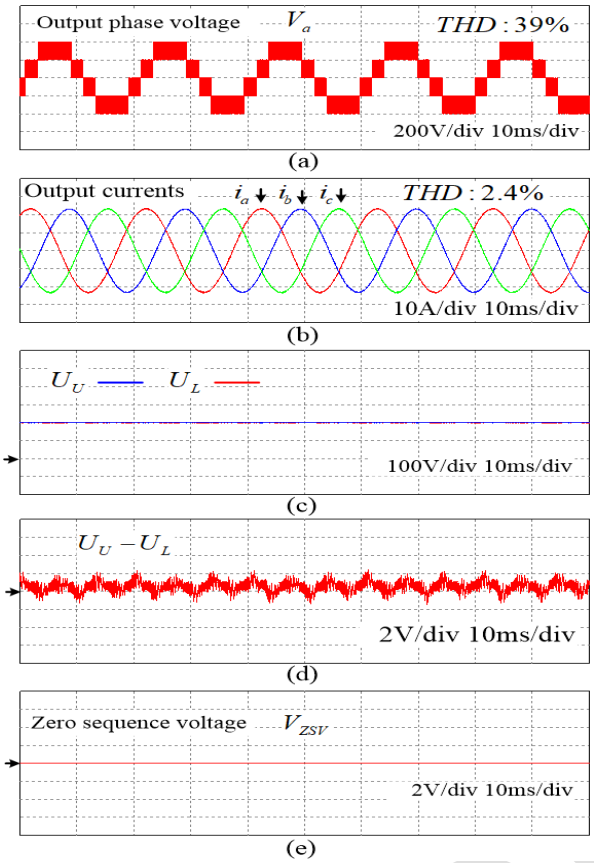

Fig. 9. Simulation results of the proposed SVM method at m = 0.8: (a), output phase voltage V_a, (b), output currents i_a, i_b, i_c, (c) capacitor voltages U_U, U_L, (d) neutral-point voltage U_U-U_L, and (e), ZSV component V_{ZSV}

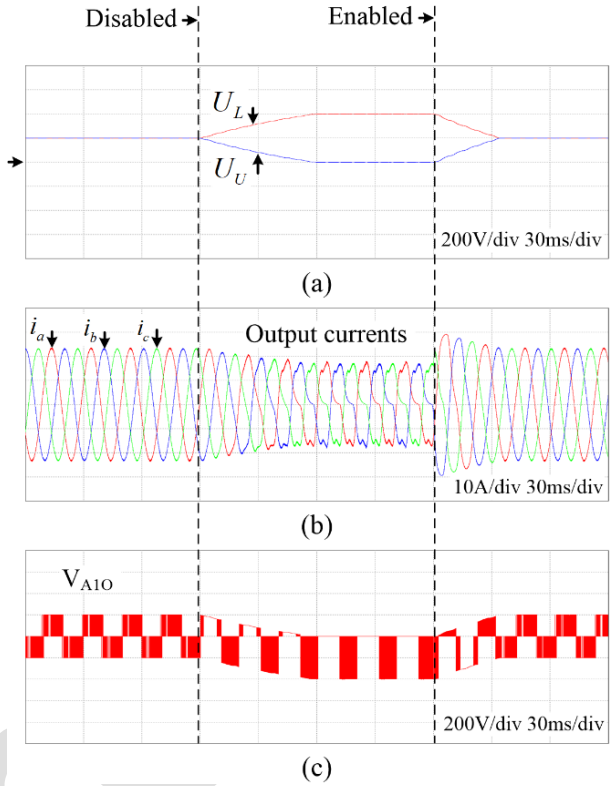

Fig. 10. Simulated performance of the proposed topology with and without the capacitor voltage balancing mechanism: (a) capacitor voltages, (b) output currents, and (c) the pole voltage V_{A1O}

To further evaluate the effectiveness of the proposed SVM method, the performance of the five-level topology at a modulation index of m = 0.8 is presented in Fig. 9. As shown in Fig. 9, the proposed SVM method effectively regulates each capacitor voltage at 200 V and successfully eliminates the ZSV component. Additionally, the number of output phase voltage steps increases to five, while the THD of the output phase voltage decreases to 39%. Furthermore, the THD of the three-phase output currents is reduced to 2.4%. These results demonstrate that the proposed SVM method effectively eliminates the ZSV component while maintaining balanced capacitor voltages in the five-level topology.

To further validate the effectiveness of the proposed modulation strategy, the performance of the inverter topology with and without the capacitor voltage balancing mechanism is illustrated in Fig. 10. During the time interval from t = 0 ms to t = 90 ms, the balancing mechanism is activated, maintaining each capacitor voltage tightly regulated at 200 V. Between t = 90 ms and t = 210 ms, the mechanism is deactivated, leading to a noticeable deviation of the capacitor voltages from their nominal values. This voltage imbalance causes distortion in the output current and a degradation in output voltage quality. Upon reactivation of the balancing mechanism at t = 210 ms, the capacitor voltages gradually return to their desired values, and both the output current waveform and output voltage levels are effectively restored.

5. Conclusion

In this paper, a novel three-phase five-level VSI topology is proposed for three-phase open-end loads. The proposed five-level VSI topology comprises 24 insulated-gate bipolar transistors (IGBTs) and eliminates the need for isolated DC sources. Additionally, the proposed topology features a competitive component count compared to other five-level VSI topologies that operate with a single DC source. Furthermore, a simplified SVM technique is introduced, which does not require the adjustment of a balancing control factor. This modulation method enables the inverter to effectively regulate capacitor voltage and eliminate the ZSV component. Simulation results demonstrate that each capacitor voltage is well maintained at one-half of the DC link voltage, and the ZSV component is effectively eliminated.

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